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Interfacing with Zynq
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Training Series:
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AXI Reference Guide
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UG761 (v13.1) March
7, 2011 How AXI Works
Figure 1-2 shows how a

Write transaction uses
the Write address,
Write data, and Write
response channels. As
shown in the preceding
figures, AXI4 provides
separate data and
address connections
for Reads and Writes,
which allows simultane-
ous, bidirectional data
transfer. AXI4

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2012 Chapter 1
Introducing AXI for
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Development
Introduction Xilinx®
adopted the Advanced
eXtensible Interface
(AXI) protocol for
Intellectual Property
(IP) cores beginning
with the Spartan®-6
and Virtex®-6 devices.
Xilinx has continued
the

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18, 2012 How AXI
Works Figure 1-2
shows how a write
transaction uses the
write address, write
data, and write
response channels. As
shown in the preceding
figures, AXI4 provides
separate data and
address connections
for reads and writes,
which allows
simultaneous ,
bidirectional data
transfer.

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Introducing AXI for
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Introduction Xilinx®

Vivado AXI Reference Guide www.xilinx.com
7 UG1037 (v3.0) June 24, 2015 Chapter 1:
Introducing AXI for Vivado Both AXI4 and AXI4-Lite interfaces consist of five different channels:

- Read Address Channel
- Write Address Channel
- Read Data Channel
- Write Data Channel
- Local Error Channel

Advanced eXensible
Interface (AXI)
Reference Guide. Xilinx

has adopted the Advanced eXtensible Interface or AXI protocol for Intellectual Protocol (IP) cores generated by their tools. This tech note provides a guide to the basic concepts on the AXI interface and some of the Xilinx IP to support it. The AXI protocol was created by ARM and is backward compatible with existing AHB and APB interfaces.

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- Updated Xilinx 04/06/2016 2016.1 Updated for Vivado 2016.1 release: • Included description of address extension, new in version 9.6. •

Included description of pipeline pause functionality, new in version 9.6 • Included description of non-secure AXI access support, new in version 9.6.

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November 15, 2012
Chapter 1 Introducing AXI for Xilinx System Development
Introduction Xilinx® adopted the Advanced eXtensible Interface (AXI) protocol for Intellectual Property (IP) cores beginning with the Spartan®-6 and Virtex®-6 devices. Xilinx continues to use of

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AXI HWICAP v3 - Xilinx

DS759 March 1, 2011
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Product Specification
LogiCORE IP AXI
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Features ... MAC User
Guide. ... used in AXI
Ethernet. Please refer
to the Reference

Documents section at
the end of document to
determine the

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The recent adoption of the AXI4 by Xilinx for all of their current and future device families and products, including the Zynq™-7000 family of Extensible Processing Platform (EPP) products, makes this protocol vital to learn for every SoC designer in order to be able to use the newest device families from major silicon vendors, and access a wide portfolio of AXI based IPs. Embracement by ...

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