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Michael Ossmann: Simple RF Circuit Design

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Figure 5.8 Single-bit TTD test results. Insertion loss from both the matched and unmatched delay circuits are compared with the loss from a straight 40Ω microstrip line. (Source: [23] ©2001 IEEE. Courtesy of Drs. R. E. Mihailovich and J. DeNatale.) - "RF MEMS Circuit Design for Wireless Communications"

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Figure 4.2 (a) Capacitive MEMS switch employed as a binary capacitor over a CPW line, and (b) binary capacitor equivalent circuit model. (Source: [8] ©2001 IEEE.) - "RF MEMS Circuit Design for Wireless Communications"

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